Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

CLAIMS

1. (Amended) A method for providing an improved integrated circuit device comprising the steps of:

providing active and passive areas in the substrate,

providing a plurality of slots in the substrate after providing the active and passive areas,

oxidizing the plurality of slots; ~~and~~

providing metal in each of the plurality of slots ~~and~~,

providing a dielectric coating over the ~~slots and the remaining silicon~~; ~~and~~

providing etched contacts in select areas remote from the location of the ~~slots buried power buss (BPB)~~; ~~and~~

providing an additional layer of metal that interconnects the contacts and the buried metal in select areas ~~where~~ around the etched contacts ~~were opened (power buss)~~, resulting in metal of three levels; and

providing one ~~layer~~ level of the metal on a top surface ~~comprising triple metal technology with one layer on the top surface consisting of a single layer of metal~~, ~~one layer that is buried comprising~~ ~~consisting of~~ and two ~~layers of a metal~~ levels of the metal that comprise a buried power buss (BPB~~), and the power buss (PB) that has three layers of metal located where contacts were opened prior to the final metal deposition; all while providing single metal processing and patterning of a single thin metal~~.

2. (Amended) The method of claim 1 wherein the ~~triple metal technology~~ providing steps comprising the step of providing three independent oxide isolated metal layers being of sufficient thickness to carry high current.

3. (Cancelled)

4. (Cancelled)

5. (Cancelled)

6. (Original) The method of claim 1 wherein active and passive areas are provided for bipolar, CMOS, BICMOS, DMOS and BCD technologies with improved properties.

7. (Amended) The method of claim 1 wherein select slots are opened in the substrate ~~dielectric~~ prior to metal to allow the oxide to be removed from the bottom of slots that are to make ground contact to the substrate and metal contact to the buried metal to replace a sinker.

8. (Cancelled)

9. (Amended) The method of claim 1 <u>wherein</u> three layers of metal are provided with only one layer of metal requiring masking and pattern etching.

10. (Cancelled)

11. (Cancelled)

12. (Cancelled)

13. (Amended) The method of claim 1 whereby the slots are ~~ideally~~ located to provide significant circuit advantages for the various technologies.

14. (Cancelled)

15. (Cancelled)

16. (Original) The method of claim 1 whereby three layers of isolated metal interconnect are formed while only requiring one layer of dielectric to be deposited and contact etched, versus standard triple metal processes which requires three layers of dielectric to be deposited and contact (or via) etched.

17. (Cancelled)

18. (Amended) The method of claim 1 whereby the high current is carried on the buried power buss (BPB) ~~and power buss (PB) with their thick metals and~~ the third layer is for interconnection of low power circuitry.

19. (Cancelled)